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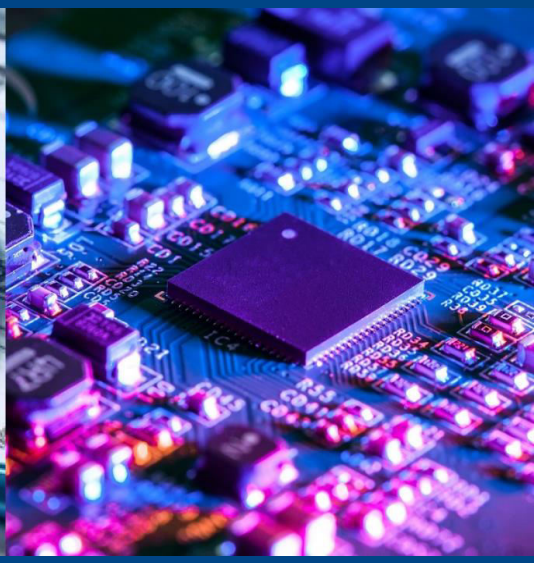

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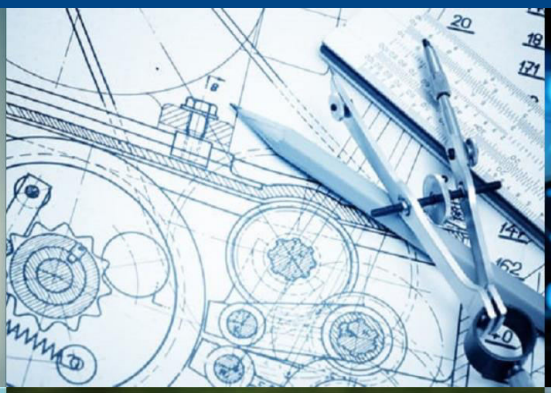

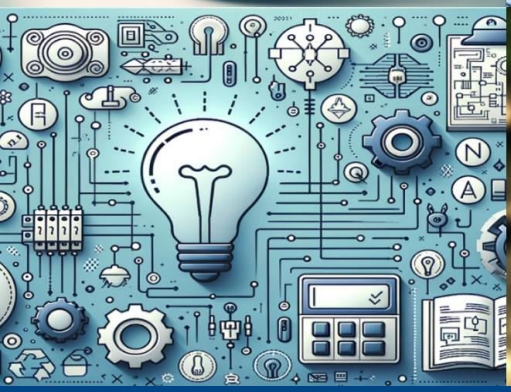

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SRAM Cell Design using FinFET for Lowpower and Delay

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ABSTRACT: Static Random Access Memory (SRAM) plays a vital role in modern high-speed and low-power electronic systems, particularly in cache memory applications. However, conventional CMOS-based 6T SRAM cells face significant challenges such as increased power consumption and delay with continuous technology scaling. This paper presents the design and analysis of a FinFET-based 6T SRAM cell aimed at improving power efficiency and reducing read/write delay. FinFET technology, with its three-dimensional structure, offers superior electrostatic control and minimizes leakage currents compared to traditional CMOS transistors.

The proposed design is implemented and simulated using Cadence tools, and a comparative analysis is carried out between CMOS (45 nm) and FinFET (18 nm) technologies. Key performance parameters such as power consumption and delay are evaluated. The results demonstrate that the FinFET-based SRAM cell significantly reduces power consumption and improves operational speed. Specifically, notable reductions in both read and write delays, along with enhanced energy efficiency, are achieved.

This work highlights the potential of FinFET technology as a promising solution for next-generation low-power, high-performance memory design, making it highly suitable for applications in mobile devices and advanced computing systems.

KEYWORDS: SRAM, 6T SRAM Cell, FinFET, CMOS, Low Power Design, Read/Write Delay, Leakage Current, LSI, Nano-scale Technology, Cadence Simulation, Memory Design, Power Optimization, High-Speed Circuits.

I. INTRODUCTION

Static Random Access Memory (SRAM) is a crucial component in modern digital systems, widely used in cache memory due to its high speed, low latency, and reliability. Among various SRAM architectures, the 6-transistor (6T) SRAM cell is the most preferred design because it offers a good balance between stability, area efficiency, and performance. It consists of two cross-coupled inverters and two access transistors, enabling efficient data storage and fast read/write operations, making it suitable for high-performance computing applications.

With continuous scaling of semiconductor technology, conventional CMOS-based SRAM cells face significant challenges such as increased leakage power, reduced noise margins, and higher read/write delays. These issues become more critical at nanoscale technologies, affecting the overall performance and energy efficiency of integrated circuits. As modern applications demand low-power and high-speed operation, especially in mobile devices and advanced processors, improving SRAM design has become a key research focus.

To overcome these limitations, FinFET (Fin Field-Effect Transistor) technology has emerged as a promising alternative to traditional CMOS. Its three-dimensional structure provides better electrostatic control, reduces leakage currents, and improves switching performance. In this paper, a FinFET-based 6T SRAM cell is designed and analyzed to achieve lower power consumption and reduced delay. The proposed design is simulated and compared with conventional CMOS SRAM, demonstrating its effectiveness for next-generation low-power, high-performance memory applications.
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II. RELATED WORK

Significant research has been conducted on improving the performance of Static Random Access Memory (SRAM) cells, particularly focusing on power reduction and delay optimization. Conventional 6T SRAM cells based on CMOS technology have been widely used due to their compact design and reliable operation. However, with continuous scaling of technology, CMOS-based SRAM cells suffer from increased leakage current, reduced noise margins, and higher read/write delays. These challenges have motivated researchers to explore alternative technologies and design approaches to enhance SRAM performance.

FinFET technology has emerged as a promising solution to overcome the limitations of traditional CMOS devices. Due to its three-dimensional structure, FinFET provides better electrostatic control over the channel, resulting in reduced leakage current and improved switching characteristics. Several studies have demonstrated that FinFET-based SRAM cells offer lower power consumption and enhanced stability compared to CMOS-based designs. Comparative analyses across different technology nodes have shown significant improvements in both energy efficiency and operational speed when FinFET technology is utilized.

In addition to adopting FinFET technology, researchers have also explored various SRAM architectures such as 7T, 8T, and other modified cell designs to improve performance metrics like stability and noise margin. Although these architectures provide certain advantages, they often increase circuit complexity and area. Therefore, the FinFET-based 6T SRAM cell remains a preferred choice, as it achieves a balanced trade-off between power, delay, stability, and design simplicity, making it suitable for modern low-power and high-speed memory applications.

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III. METHODOLOGY

The proposed work focuses on the design and analysis of a 6T SRAM cell using FinFET technology to achieve low power consumption and reduced delay. The conventional 6T SRAM cell structure, consisting of two cross-coupled inverters and two access transistors, is implemented using FinFET devices instead of traditional CMOS transistors. The FinFET-based design leverages its three-dimensional structure to provide improved electrostatic control, thereby minimizing leakage currents and enhancing switching performance. The basic operations of the SRAM cell, including hold, read, and write modes, are carefully designed and verified.

The implementation and simulation of the proposed SRAM cell are carried out using Cadence design tools. Two different technologies are considered for comparison: CMOS technology at 45 nm with a supply voltage of 1 V, and FinFET technology at 18 nm with a reduced supply voltage of 0.5 V. The SRAM cell is designed, and its functionality is validated through transient analysis. Key performance parameters such as power consumption and read/write delay are measured under both technologies to evaluate the effectiveness of the FinFET-based design.

A comparative analysis is performed between CMOS-based and FinFET-based SRAM cells to assess improvements in performance. Simulation results are analyzed to determine reductions in power dissipation and delay. The results demonstrate that the FinFET-based SRAM cell achieves significant improvements in energy efficiency and speed due to reduced leakage current and better control over short-channel effects. This methodology provides a systematic approach for evaluating advanced transistor technologies in modern memory design.

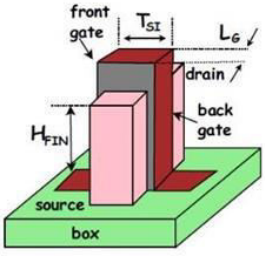

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Fig 1 Typical n/p FinFET Device

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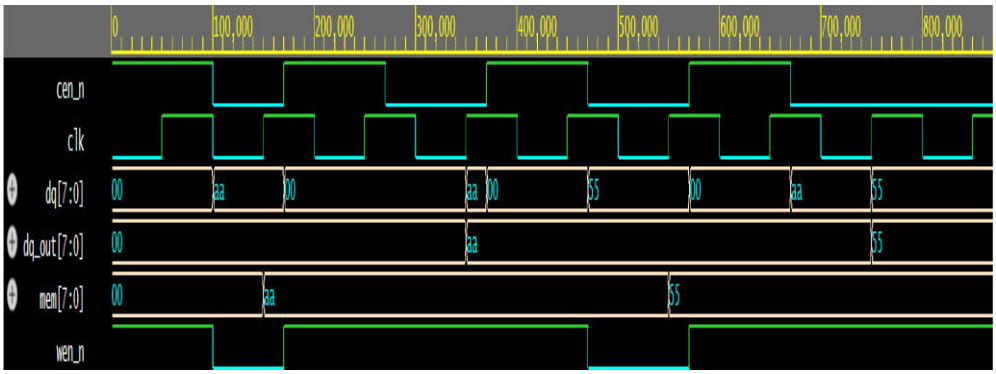
IV.EXPERIMENTAL RESULTS

The proposed 6T SRAM cell using FinFET technology was designed and simulated using Cadence tools to evaluate its performance in terms of power consumption and delay. For comparison, a conventional CMOS-based 6T SRAM cell was also implemented. The CMOS design was analyzed at 45 nm technology with a supply voltage of 1 V, while the FinFET-based design was evaluated at 18 nm technology with a reduced supply voltage of 0.5 V. Transient simulations were carried out to verify the functionality of the SRAM cell during hold, read, and write operations.

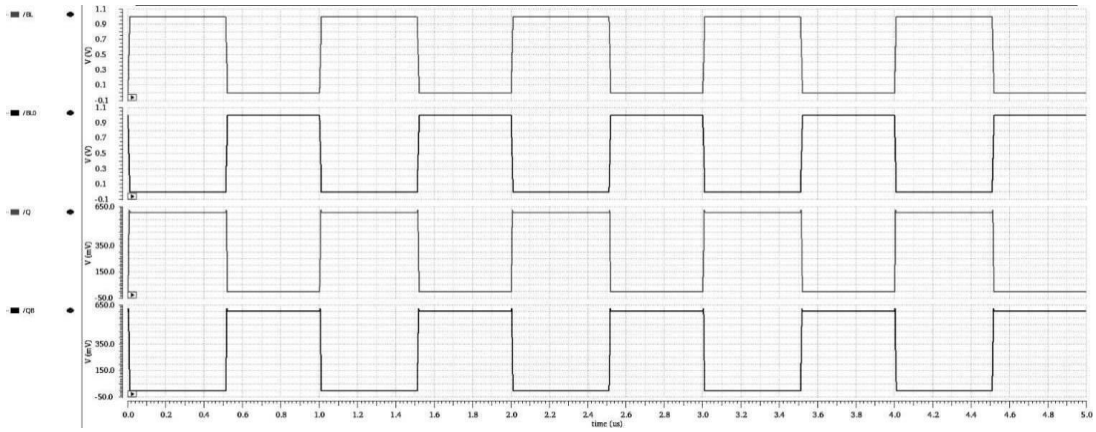
The simulation results indicate a significant improvement in performance when using FinFET technology. The power consumption of the CMOS inverter was observed to be 537.93 nW, whereas the FinFET inverter consumed only 12.512 nW. Similarly, in the SRAM cell, CMOS-based design exhibited a power consumption of 7.38 µW, while the FinFET-based SRAM consumed only 2.71 µW. In terms of delay, the CMOS SRAM showed a write delay of 4.429 ms and a read delay of 4.427 ms, whereas the FinFET SRAM achieved a reduced write delay of 0.508 ms and read delay of 0.878 ms.

These results clearly demonstrate that the FinFET-based 6T SRAM cell provides substantial improvements in both power efficiency and operational speed compared to the conventional CMOS design. The reduction in leakage current and enhanced electrostatic control in FinFET devices contribute significantly to these improvements. Therefore, the proposed FinFET SRAM design is well-suited for low-power and high-performance applications in advanced VLSI systems.

Fig 2:



a. simulation results



b. Write operation

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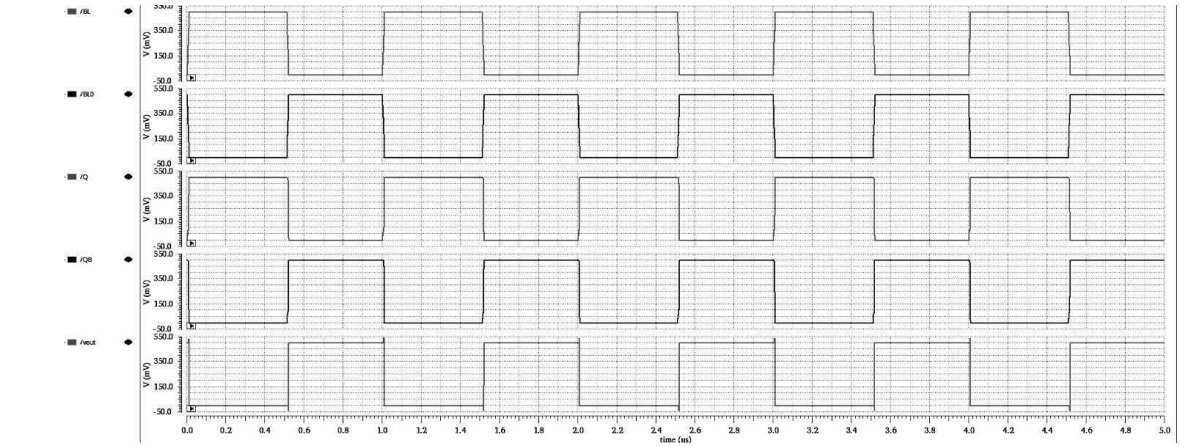

c. Read Operation

Fig 2 Shows Results (a) Simulation Results ,(b) write Operation ,(c) Read Operation

V. CONCLUSION

In this paper, a FinFET-based 6T SRAM cell has been designed and analyzed to address the challenges of high power consumption and delay in conventional CMOS-based SRAM designs. By leveraging the three-dimensional structure of FinFET technology, the proposed design achieves improved electrostatic control, reduced leakage current, and enhanced switching performance. The implementation and simulation were carried out using Cadence tools, and a comparative analysis was performed between CMOS (45 nm) and FinFET (18 nm) technologies.

The experimental results demonstrate that the FinFET-based SRAM cell significantly reduces power consumption and read/write delay compared to the conventional CMOS design. The observed improvements highlight the effectiveness of FinFET technology in achieving better energy efficiency and faster operation, making it suitable for modern high-speed and low-power applications. The reduction in supply voltage and minimized short-channel effects further contribute to the overall performance enhancement.

Overall, the proposed FinFET-based 6T SRAM cell proves to be a promising solution for next-generation memory design in VLSI systems. Future work can focus on further optimization of the design, exploration of advanced SRAM architectures, and analysis under different process variations to enhance stability and reliability.

REFERENCES

[1]S. Priyanka, M. Raheez, “Design and examination of 6T SRAM in 45nm Technology”, in international journal of Engineering Research and Technology (IJERT)
[2]Deepika Sharma, “A Review on SRAM Design Using CMOS and FinfET”, in International Journal of Research and Analytical Reviews (IJRAR)
[3]Rohit Kumar Sah, “Performance Analysis of a 6T SRAM Cell in 180nm CMOS Technology”, in North Eastern Regional Institute of Science and Technology, Nirjuli, India
[4]Shikha Saun, Hemant Kumar, “Design and Performance analysis of 6T SRAM Cell on different CMOS Technologies with Stability Characterisation”, in Department of Electronics, Banasthali Vidyapith, Rajasthan, india
[5]Abhishek Agal, Pradeep, Bal Krishan, “6T SRAM Cell Design and Analysis”, in Electronics Engineering Department,
YMCA University of science & technology, Faridabad
[6]Meenakshi Devi, Charu Madhu, Nidhi Garg, “Design and analysis of CMOS based 6T SRAM cell at different technology nodes”, in Electronics and Communication Department, University Institute of Engineering and Technology (UIET), Panjab University, Chandigarh 160025, India

ISSN: 2582-7219 | www.ijmrset.com | Impact Factor: 8.206| ESTD Year: 2018|

International Journal of Multidisciplinary Research in Science, Engineering and Technology (IJMRSET)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

[7]Gurmohan Singh, "FinFET based 6T SRAM Cell for Nanoscaled Technologies", in International Journal of Computer Applications

[8]Shivani Yadav, Neha Malik, Ashutosh Gupta and Sachin Rajput, "Low Power SRAM Design with Reduced Read/Write Time", in Dept. of ECE, Amity University Noida Sector-125, India.

[9]K.Dhanumjaya, "Design of Low Power SRAM in 45 nm CMOS Technology", in JNTU Anantapur,AP, India.

[10]Ms. M. S. Mhaske, Mr. P. B. Vikhe, Prof. S. A. Shaikh, "analysis of 6t sram cell using finfet at nanometer regime", in Novateur Publication's International Journal of Innovation in Engineering, Research and Technology [IJIERT], ICITDCEME'15 Conference Proceedings, ISSN No - 2394-3696.

[11]Mr.S.Mohammed Sulaiman, B.Jaison, M.Anto Bennet, M.Vijay, V.Pandi Selvam, P.Anandakumar, "design of sram architecture with low power without affecting speed using finfet", in international journal on smart sensing and intelligent systems special issue, september 2017.

[12]Syed Samsuz Zaman, Pankaj Kumar, Manash Pratim Sarma, Ashok Ray and Gaurav Trivedi, "Design and Simulation of SF-FinFET and SD-FinFET and Their Performance in Analog, RF and Digital applications" in 2017 IEEE International Symposium on Nanoelectronic and Information Systems.

[13]Sourindra Chaudhuri, Niraj K. Jha, "finfet logic circuit optimization with different finfet styles: lower power possible at higher supply voltage", in 2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems.

[14]Jigyasa panchal, Dr.Vishal Ramola, "design and implementation of 6t sram using finfet technology for low-power operation" in International Research Journal of Engineering and Technology (IRJET),

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